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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,447	03/01/2004	Nobuaki Hashimoto	118890	9995

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
AU, BAC H	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,447	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	Bac H. Au	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *8-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01 March 2004*; 9/19/05; 6/15/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated June 2, 2006 in which claims 1 and 3-5 were amended has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuneo (JP-A-09-051020).

Regarding claims 1-7, Tsuneo [Figs.1-5] discloses a method of manufacturing an electronic device, the method comprising:

forming an external terminal [21] on an interconnect pattern formed on a substrate [2];

subsequently mounting a chip component [3] on the substrate face up, the chip component having an electrode [10] on a first surface of the chip component [Para.30 lines 4-6] opposite a second surface facing the substrate;

forming an insulating section [19,11] adjacent to the chip component; and

forming an interconnect [12] on the insulating section from the electrode [10] to the interconnect pattern [5] for electrically connecting the electrode and the interconnect pattern at a temperature lower than a melting point of the external terminal [As disclosed (Paras.41-47 and process steps as described in Figs.2-5), whereby the external terminals 21 are formed on the substrate prior to the mounting of chip 3 and forming of interconnect 12. For this reason, it would be inherent that the process of forming the interconnect (curing of a conductive paste in this case) is done below the melting point of the external terminals in order to not cause damage to the external terminals 21.];

wherein the interconnect [12] is formed of a dispersant including electrically conductive particles [Para.47];

wherein the step of forming the interconnect includes ejecting a dispersant including the electrically conductive particles over the insulating section and the interconnect pattern [Para.47];

wherein the insulating section is formed of a resin [Para.46];

wherein the insulating section is formed to have an inclined surface descending in an outward direction from the chip component [Fig.4];

wherein the chip component is a semiconductor element [Para.44].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo (U.S. Pat. 5550408) in view of Horiuchi (U.S. Pat. 6084295).

Regarding claim 1, Kunitomo discloses a method of manufacturing an electronic device, the method comprising:

forming an external terminal [15 of Fig.9] on an interconnect pattern formed on a substrate [Col.5, lines 8-12];

subsequently mounting a chip component [Shown in Fig.9 (labeled as 10 of Fig.3)] on the substrate, the chip component having an electrode [16 of Fig.9] on a first surface of the chip component opposite a second surface facing the substrate;

forming an insulating section adjacent to the chip component [14 of Fig.9; col.6, lines 3-6]; and

forming an interconnect [17 of Fig.9] on the insulating section from the electrode to the interconnect pattern for electrically connecting the electrode and the interconnect pattern at a temperature lower than a melting point of the external terminal [As disclosed (Col.9, lines 45-52, whereby the manufacture of the insulating substrate is completed after the formation of external terminals 15, made of high melting point solder

balls; as well as the sequence of the process steps as described in Figs. 6-9), the external terminals 15 are formed on the substrate prior to mounting the chip, and then the subsequent forming of the interconnect 17. For this reason, it would be inherent that the process of forming the interconnect (curing of an ultraviolet-curing ink in this case) is done below the melting point of the external terminals in order to not cause damage to the external terminals 15.].

Regarding claim 2, Kunitomo discloses wherein the interconnect [17] is formed of a dispersant including electrically conductive particles [Col.8, lines 56-64].

Regarding claim 3, Kunitomo discloses:

wherein the step of forming the interconnect includes ejecting a dispersant including the electrically conductive particles over the insulating section and the interconnect pattern [17 of Fig.9; col.8, lines 56-64].

Regarding claims 4-6, Kunitomo discloses wherein the insulating section is formed of a resin [Col.6, lines 3-6];

wherein the insulating section is formed to have an inclined surface descending in an outward direction from the chip component [14 of Fig.9].

Regarding claim 7, Kunitomo [Col.5, lines 53-59] discloses wherein the chip component is a semiconductor element.

Kunitomo fails to disclose in claim 1 wherein a chip component is mounted on the substrate **face up**. However, Horiuchi [Fig.1] discloses wherein a chip component [10] is mounted face up on the substrate [5].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Kunitomo into the method of Horiuchi to mount a chip component face up on the substrate.

The ordinary artisan would have been motivated to modify Kunitomo in the manner set forth above for at least the purpose of providing a package without the need for a build-up layer that is low cost and higher in reliability [Horiuchi; Col.1 lines 49-53].

Response to Arguments

4. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BHA

Zandra V. Smith
Supervisory Patent Examiner
19 June 2006